



Introduction to ClearSpeed Acceleration

ClearSpeed Technology Plc.

Overview

- **Course aims**
- **Background to ClearSpeed Technology**
- **What is an accelerator?**
- **What can be accelerated?**
- **What this course contains**
- **Further reading**
- **ClearSpeed Developer Program**



Course Aims

Course Aims

“To enable the reader to get optimal performance for their application with ClearSpeed accelerators”

- **Achieve this by covering the ClearSpeed:**
 - Architecture
 - Programming model
 - Tools
 - Optimization techniques



Background to ClearSpeed Technology

Background to ClearSpeed Technology

- **ClearSpeed founded in 2001**
 - Focus on alleviating the power, heat, and density challenges of HPC systems
 - Offices in San Jose, California and Bristol, UK

ClearSpeed Technology: Products

- **ClearSpeed Advance Accelerator cards**
 - X620 and e620 (PCI-X and PCI Express interfaces)
 - both contain dual CSX600 accelerators
 - 80.64 GFLOPS peak double precision performance
- **Software environment**
 - full toolchain (Cⁿ compiler, assembler, linker)
 - Visual profiler, gdb-based debugger
 - CSXL, CSDFT acceleration libraries
- **Applications supported**
 - Amber Implicit
 - interactive Supercomputing's Star-P
 - Mathematica
 - MATLAB
 - many more applications under development



What is an accelerator?

What is an accelerator?

- **A device to improve performance**
 - relieve main CPU of workload
 - or to augment CPU's capability

- **An accelerator card can increase performance**
 - on specific tasks
 - *without* aggravating facility limits on clusters (power, size, cooling)

All accelerators are good... *for their intended purpose*

FPGAs

- Good for integer, bit-level ops
- Programming looks like circuit design
- Low power per chip, but
20x more power than custom VLSI
- Not for 64-bit FLOPS

Cell and GPUs

- Good for video gaming tasks
- 32-bit FLOPS, not IEEE
- Unconventional programming model
- Small local memory
- High power consumption (> 200 W)

ClearSpeed

- Good for HPC applications
- IEEE 64-bit and 32-bit FLOPS
- Custom VLSI, true coprocessor
- At least 1 GB local memory
- Very low power consumption (25 W)
- Familiar programming model

The case for accelerators

- **Accelerators designed for HPC applications can improve performance as well as performance per (watt, cabinet, dollar)**
- **Accelerators enable:**
 - larger problems for given compute time, or
 - higher accuracy for given compute time, or
 - same problem in shorter time
- **Host to card latency and bandwidth are not major barriers to successful use of properly designed accelerators.**

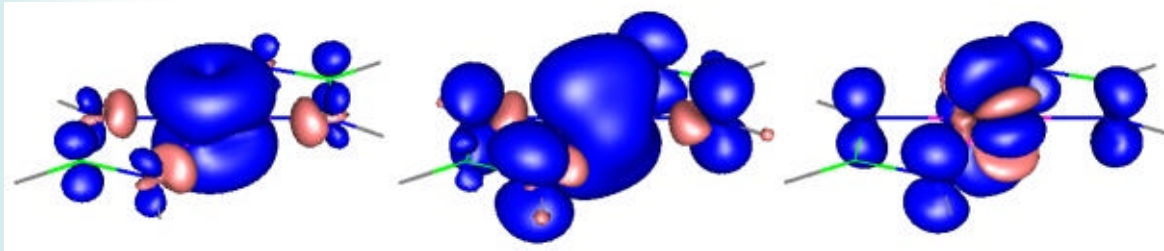


What can be accelerated?

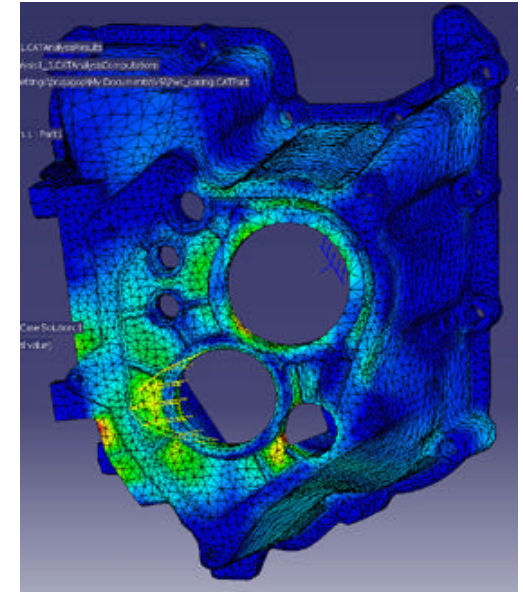
Good application targets for acceleration

- **Application needs to be both *computationally intensive* and contain a high degree of *data parallelism***
- ***Computationally intensive:***
 - software depends on executing large numbers of arithmetic calculations
 - usually 64-bit floating point operations (FLOPS)
 - should also have a high ratio of FLOPS to data movement (bandwidth)
 - computationally intensive applications may run for many hours or more, even on large clusters
- ***Data parallelism:***
 - software performs the same sequence of operations again and again but on a different item of data each time
- **Example computationally intensive, data parallel problems include:**
 - large matrix arithmetic (linear algebra)
 - molecular simulations
 - Monte Carlo options pricing in financial applications
 - and many, many more...

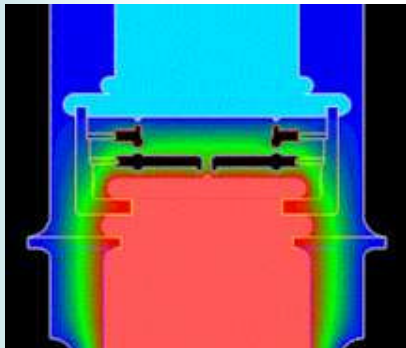
Example data parallel problems that can be accelerated



Ab initio Computational Chemistry



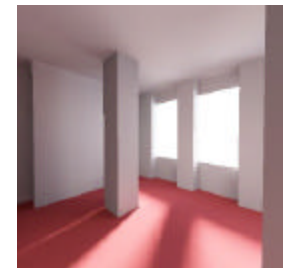
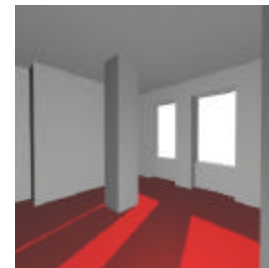
Structural Analysis



Electromagnetic Modeling

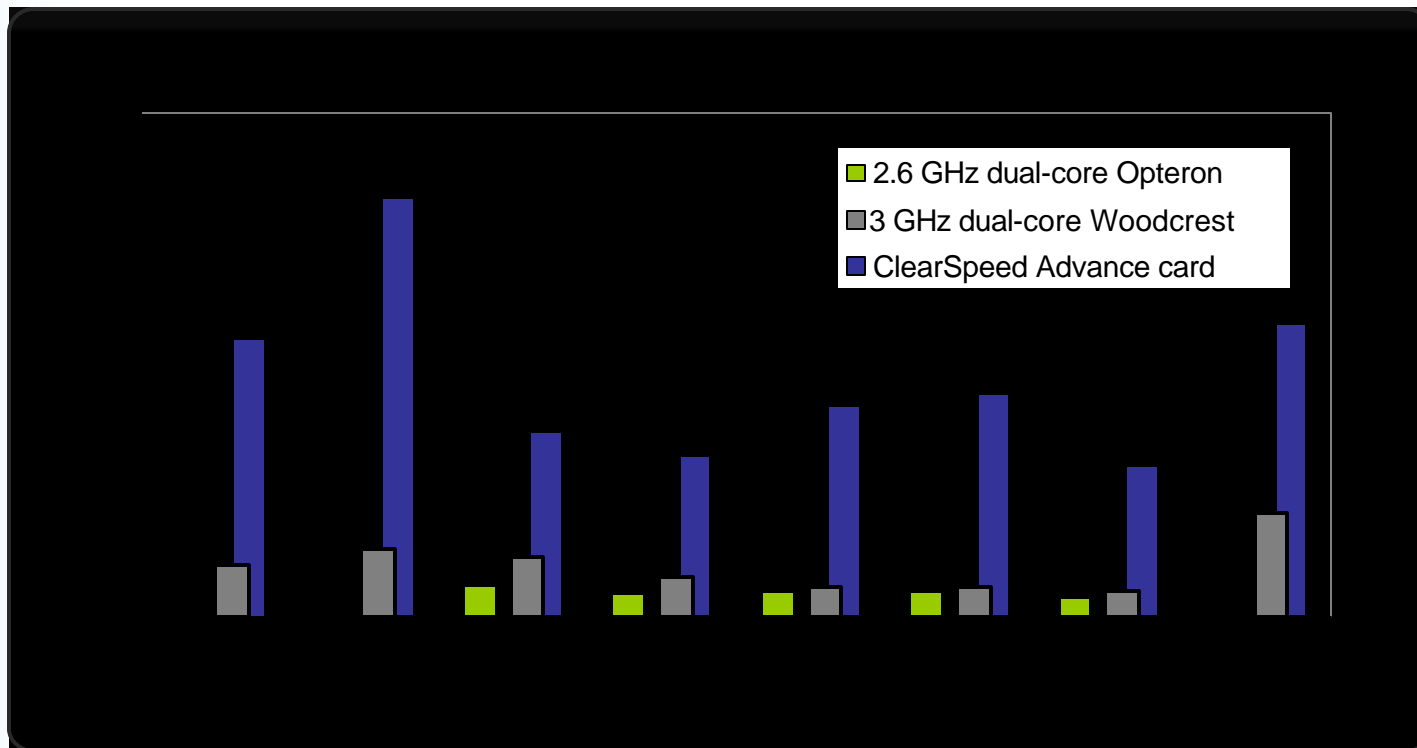


Radar Cross-Section



Global Illumination Graphics

Acceleration example: math function speed



- ClearSpeed's accelerators come with optimized math libraries to aid in porting applications
- All performances are vendors' own peak figures: Opteron figure is for optimal ACML performance, Woodcrest figure is optimal MKL figure. All figures are from running on long vectors in on-chip cache or poly mem.

Plug and play acceleration

- **CSXL is ClearSpeed's host-side library**
 - provides some of the most commonly used and important Level 3 BLAS and LAPACK functions
 - exploits standard shared/dynamic library mechanisms to intercept calls to L3 BLAS and LAPACK
 - can execute calls heterogeneously across both the multi-core host and the ClearSpeed accelerators simultaneously for maximum system performance
 - compatible with ACML from AMD and MKL from Intel amongst others
- **In the “plug and play” model the application does not need to be explicitly aware of the acceleration hardware**
 - except that the application suddenly runs faster...



What this course contains

What this course contains

- **Course modules:**
 - Overview of Architecture: Host and ClearSpeed
 - ClearSpeed Programming Model: Introduction
 - Introduction to Parallel Programming
 - ClearSpeed Programming Model: Board Side Libraries
 - ClearSpeed Programming Model: Case Study
 - ClearSpeed Programming Model: Optimising Performance
- **Learn by example**
- **Top-down approach**



Further reading

Document installed with the ClearSpeed SDK

- **Can be found inside the “docs” directory:**
 - CSXL User Guide
 - Runtime User Guide
 - Visual Profiler User Guide with additional worked examples
 - SDK documentation
 - Introductory Programming Guide
 - SDK Reference Manual
 - Debugging with GDB
 - Cⁿ Standard Libraries
 - Instruction Set Reference Manual
 - Release notes
- **Also source code examples in the “examples” directory**

Online documentation

- **All available from the ClearSpeed Support Website**
- **<http://support.clearspeed.com/documentation/>**
- **All currently released General Availability (GA) documentation available for download in PDF form**

ClearSpeed online

- **General information, news, and so on**
 - company website www.clearspeed.com
- **Report a problem, find answers**
 - support website support.clearspeed.com
- **Support website has:**
 - documentation, user guides, reference manuals
 - solutions knowledge base
 - software downloads
 - log a case



ClearSpeed Developer Program

Join the ClearSpeed Developer Program!

- **Designed to support the leading-edge community of developers using accelerators**
- **Membership is free and has the following benefits:**
 - access to the ClearSpeed Developer website
 - ClearSpeed Developer Community on-line forum
 - invitations to participate in ClearSpeed Developer and User Community meetings and events
 - repository to share and access demonstrations and sample codes within the ClearSpeed Developer Community
 - technical updates, tips and tricks from the gurus at ClearSpeed and the Developer Community
 - and more, including opportunities to preview new software releases and developer discount programs
- **Leverage the expertise of developers worldwide**
- **Ask a question, or share your knowledge**
- **Register now at developer.clearspeed.com !**



Summary

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- **Introduced ClearSpeed Technology**
- **What is an accelerator**
- **What can be accelerated**
- **What the course modules contain**
- **Further reading**
- **Developer program**

ClearSpeed™