



Real Science
Real Numbers
Real Software



Welcome to the 2nd ClearSpeed User Group (CSUG) Meeting

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VP of Customer Applications

ISC08, June 16th 2008

Agenda

| | |
|----------------------|---|
| 8:30 – 9:15 | Registration and Breakfast |
| 9:15 – 9:30 | Welcome |
| 9:30 – 10:00 | <i>ClearSpeed Roadmap and New Products</i>, Simon McIntosh-Smith |
| 10:00 – 10:30 | <i>ClearSpeed Acceleration Applied to Passive Coherent Location</i>, Dr Khomotso Kganyago, Centre for High Performance Computing, South Africa |
| 10:30 – 10:45 | Break |
| 10:45 – 11:15 | <i>Accelerator Enabling Program</i>, Bill Brown, SGI |
| 11:15 – 11:45 | <i>IMSL Numerical Libraries Accelerated with the ClearSpeed Advance Accelerators</i>, Tim Leite, Visual Numerics, Inc. |
| 11:45 – 12:15 | <i>BUDE: Accelerating a Molecular Docking Program on ClearSpeed</i> Dr Richard Sessions, University of Bristol |
| 12:15 – 1:15 | Lunch |
| 1:15 – 1:45 | <i>The Method of Moments: The Perfect ClearSpeed Application</i>, Tim Lanfear, ClearSpeed Technology |
| 1:45 – 2:15 | <i>Productivity Solution for ClearSpeed Accelerators</i>, Dave Gibson, Interactive Supercomputing |
| 2:15 – 2:45 | <i>Experiences in a ClearSpeed Multi-card Environment</i>, Dr Thomas Steinke, ZIB |
| 2:45 – 3:00 | <i>The Future of SuperComputing: Practical PetaFLOPS</i>, Simon McIntosh-Smith, ClearSpeed Technology |
| 3:00 – 4:30 | Beer Garden Social Hour |



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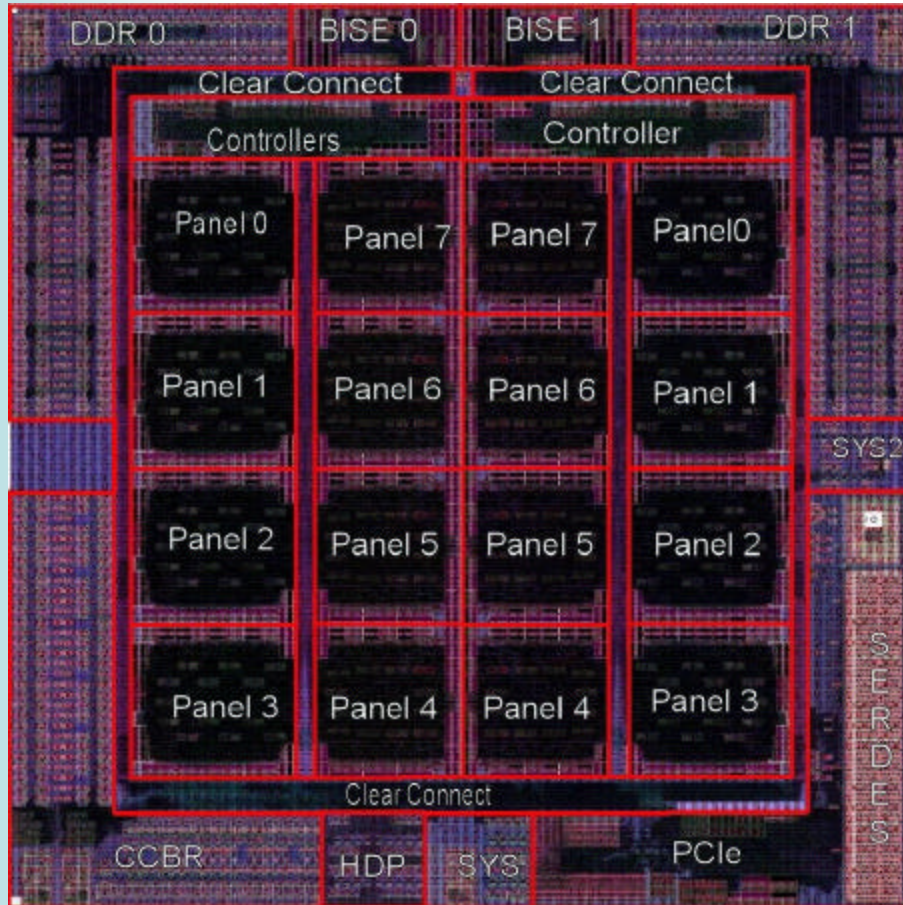
June 17th 2008 News

**Introducing ClearSpeed's latest HPC accelerator:
The CSX700 "Callanish" processor**

The CSX700 – an accelerator designed for HPC

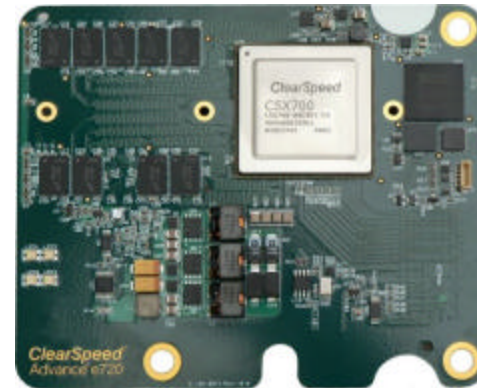
- **ClearSpeed is the only company designing accelerators specifically for HPC:**
 - Focus on 64-bit double precision for high accuracy
 - High reliability features designed in
 - Low power combined with high performance per watt
 - Form factors to fit into the standard blades and servers that populate large datacenters
- **The CSX700 is the latest accelerator from ClearSpeed, delivering big increases in:**
 - Performance,
 - Performance per dollar, and
 - Performance per watt

The CSX700 – “Callanish”



- **Processor Cores:**
 - 192 Processor Elements (2x96)
 - 96 double precision GFLOPS
 - 250MHz
 - 8 redundant PEs
 - Error Correction (ECC) on all internal memories
- **SoC details:**
 - Integrated PCI Express x16
 - 2x integrated ECC DDR2 memory controller + scrubber
 - 2x128 KBytes of SRAM
- **Design details:**
 - IBM 90nm process
 - 256 million transistors
- **12W Max (Power Managed)**
- **Officially launching at ISC08**

The ClearSpeed Advance™ e710 & e720 accelerators



- **Enterprise-class HPC accelerators**
- **The *only* accelerators designed to fit into most standard servers and blades**
 - Low power consumption – 25W max; small, light
- **Designed for high reliability (MTBF)**
 - *All* memory is error protected; no moving parts needed (e.g. fans)
- **96 Double Precision (D.P.) IEEE 754 GFLOPS peak**
 - ~4 GFLOPS per watt double precision
- **Over 2 GBytes/s between accelerator and host – PCIe x8**
- **No extra power connectors, cooling or space/slots required**
- **Launching at ISC08**

The ClearSpeed Accelerated Terascale System

CATS-700 launching at ISC08



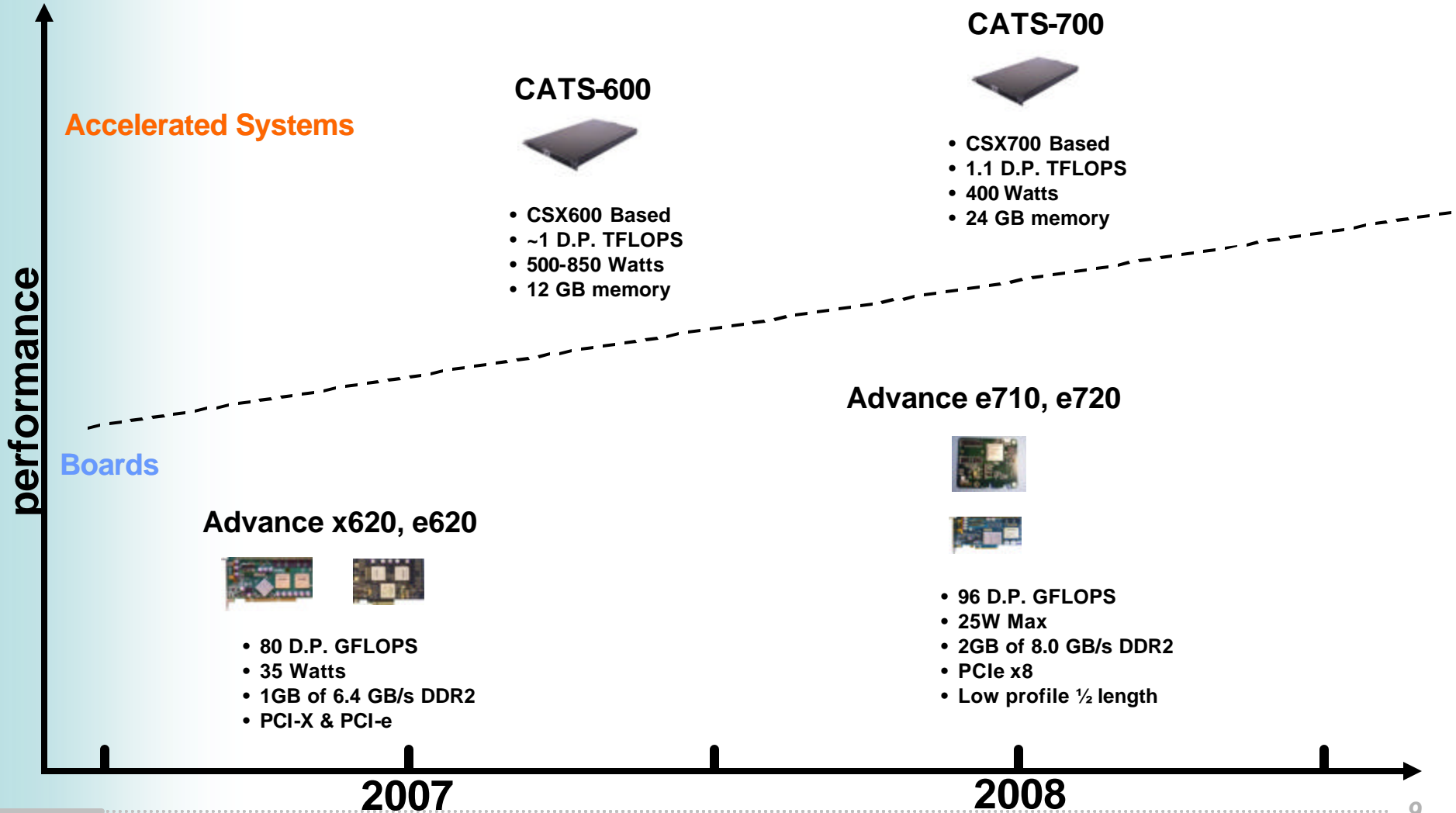
- **Enterprise-class reliability:**
 - Error correct/detect on *all* memories
 - Error correct/detect on *all* communications
- **1.152 TFLOPS double precision (64-bit) in 1U**
- **12 Advance™ e710 accelerators**
- **24 GBytes of DDR2 DRAM with SECDED ECC and Scrub**
- **96 GBytes/s of DRAM bandwidth**
- **400 watts typical power consumption**
- **Two PCI Express x8 connections to the host (up to 3m long)**
- **Up to 41 TFLOPS double precision peak in a single rack**
 - From 36 CATS-700 1U nodes
- **10X greater peak performance than the fastest dual socket 3GHz quad-core servers at the *same* power consumption**

A rack of CATS-700



- Enterprise-class reliability – ECC on *all* memories, both on- and off-chip
- From 18 CATS-700:
 - 20.7 TFLOPS double precision
 - 432 GBytes of DDR2 with ECC
 - 1.73 TBytes/s of DRAM bandwidth
 - 7.2 KW typical power consumption
- From 18 3GHz quad core hosts:
 - 1.8 TFLOPS double precision
 - 7.2 KW typical power consumption
- **22.5 TFLOPS double precision total**
- **14.4 KW total power consumption**
- No silent software errors

Product Line Overview



New software development environment for CSX700

- **Version 3.10 beta release at ISC**
- **Binary compatible across all ClearSpeed products**
 - The same executables run on the CSX700 and CSX600
- **Cⁿ optimising compiler**
 - C with **poly** extension for SIMD datatypes
 - Uses mature ACE CoSy compiler development system
 - Generates performance within 90% of hand optimized performance on many codes
- **Debugger – a port of gdb**
 - *Runs on ClearSpeed's hardware at full speed*
- **Profiling – csprof**
 - Heterogeneous, system-wide visualisation of an accelerated application's performance while running on both a multi-core host and ClearSpeed accelerators. *ClearSpeed's hardware can be profiled in real-time*
- **Libraries (BLAS, RNG, FFT, more...) & High level APIs – CSPX**
- **Preview of an ECLIPSE IDE**



Easy to use – porting code to ClearSpeed

Example from Asian Option Monte Carlo example – the original code is on the left, the ClearSpeed optimized version is on the right. The Cn code uses the new vector type operator overloading.

```
double x, y, ... ;

for (j = 0 ; j < Inputs.NumIntervals ; j++)
{
    /*
     * x,y = gaussian random pair
     */
    gaussrandv(&rngstream, &x, &y);

    Spath1    *= exp(drift + x * diffusion);
    arithave1 += Spath1;
    geoave1   += log(Spath1);

    Spath2    *= exp(drift + y * diffusion);
    arithave2 += Spath2;
    geoave2   += log(Spath2);
}
```

```
__DVECTOR x, y, ... ;

for (j = 0 ; j < Inputs.NumIntervals ; j++)
{
    /*
     * x,y = gaussian random pair
     */
    gaussrandv(&rngstream, &x, &y);

    Spath1    *= cs_expp(drift + x * diffusion);
    arithave1 += Spath1;
    geoave1   += cs_logp(Spath1);

    Spath2    *= cs_expp(drift + y * diffusion);
    arithave2 += Spath2;
    geoave2   += cs_logp(Spath2);
}
```

Eclipse IDE – CSX Debug Perspective



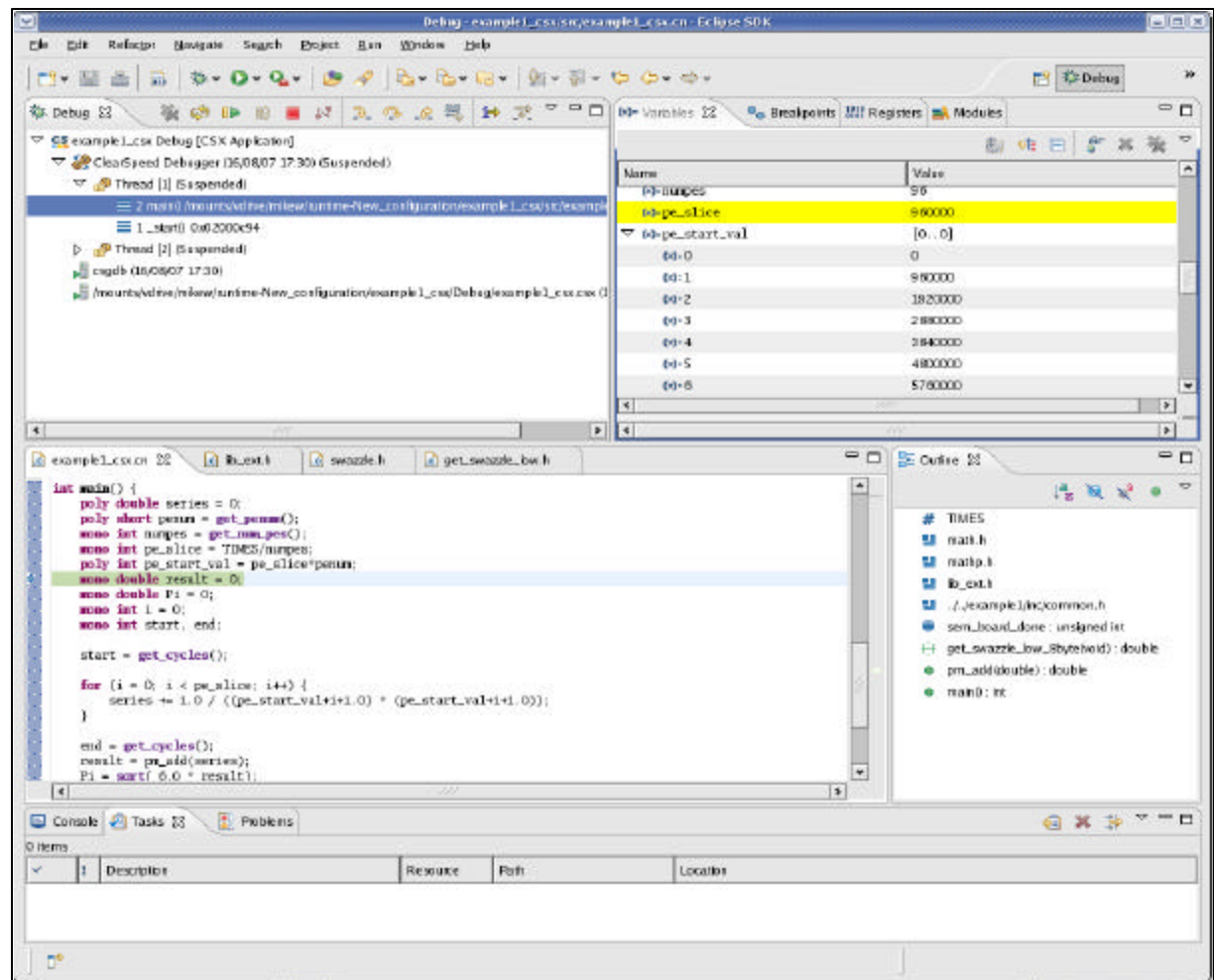
Standard Eclipse graphical debug interface for CSX processor debugging.

CSX processor provides full hardware debugging of application code.

Provides seamless view of all PEs and their associated state.

Allows full symbolic debug of the Cⁿ language.

Enhanced views for CSX specific information.



Developer support

- **Lots of online support and self-training materials:**
 - <http://developer.clearspeed.com/resources/training/>
 - Self-paced training for programmers, includes optimisation tips
 - <http://developer.clearspeed.com>
 - Online manuals, training materials, forums, support
 - <http://support.clearspeed.com>
 - All the latest software downloads, including example codes

Partners



AMBER



INTERACTIVE
supercomputing

multipath

nag

Visual Numerics

WOLFRAMRESEARCH
www.wolfram.com

excelian

NE | NISSHO
ELECTRONICS

 Super Sonic Technology Ltd

Tao
Computing

Summary

- **ClearSpeed is introducing a brand new range of accelerators based on the new CSX700 including the e710, e720 and CATS-700:**
 - The *only* accelerators designed specifically for HPC from the ground up
 - Big increases in performance, performance per dollar *and* performance per watt
 - The only accelerators delivering *Enterprise-class* features to enable reliable Petascale systems
- **The CSX700's compelling performance and extremely low power also opens up opportunities in embedded processor markets**

“Acceleration you can count on, results you can trust”

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